



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,454	11/17/2003	David Hennah Mansell	550-485	2292
23117	7590	12/14/2005	EXAMINER	
NIXON & VANDERHYE, PC			SCHLIE, PAUL W	
901 NORTH GLEBE ROAD, 11TH FLOOR				
ARLINGTON, VA 22203			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,454	MANSELL ET AL.	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 11/17/03.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-51 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-51 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 01 April 2004 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 - Certified copies of the priority documents have been received in Application No. _____.
 - Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. Claims 1-51 have been examined.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 1 and 34 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Motorola "M68040 User's Manual".

As per claim 1 and 34, Motorola teaches a data processing apparatus and corresponding enabling methods comprising: a processor operable in both non-secure mode and secure modes (i.e. user/supervisor modes), such that when executing a program in non-secure mode, the processor may be restricted from accessing data otherwise accessible when executing in secure mode; an MMU which converts a requested virtual addresses to a corresponding physical address; and corresponding page tables utilized in the process comprising: a first set of tables containing a number of descriptors, each containing at least a virtual address portion and a corresponding intermediate address portion; and a second set of tables containing descriptors comprising at least a physical address portion, where the second set of tables may be prohibited from being managed by the processor in non-secure mode (see Section 1.6 Programming Model, and Section 3 Memory Management Unit). Where although the reference's terminology differs from that used in the claims, the two are effectively

logically equivalent, and while the second set of page tables taught by the reference does not explicitly contain an intermediate address portion, it's implied by it's own address, therefore correspondingly unnecessary to be stored explicitly.

4. Claims 2-6, 22-33, 35-39, and 44-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motorola "M68040 User's Manual" in further view of Chauvel et al. (US App. Pub. No. 2002/0073282).

As per claims 2-6, 22-33, 35-39, and 44-51, being dependant on claim 1, 34, or correspondingly dependant claim inclusively, Motorola further teaches a monitor mode being a secure mode (i.e. supervisor mode) which correspondingly gates access to both secure mode code and data through exclusive access to page table control resources and descriptor mapping, thereby enabled to establish any arbitrary virtual to physical mapping of both the page tables and/or data regions they correspondingly control secure and/or non-secure access to, as may be correspondingly associated with any arbitrary process operating within either secure or non-secure mode itself, inclusive of operating systems; but does not explicitly teach that a micro-TLB may be utilized to improve the performance efficiency of the translation process and contain descriptors merged from both first and second page tables, or that it may be flushed when the mode of the processor changes between secure and non-secure modes of operation. However, Chauvel et al. teaches this (see figures 2A/B-3, and lines 13-18 of the abstract). It would be obvious to one of ordinary skill in the art at the time of the disclosed invention to combine that taught by Motorola with that taught by Chauvel et al. relevant to these claims, for the benefit of constructing a data processing apparatus

capable of efficiently supporting both secure and non-secure mode processing. Any and all potentially further remaining claimed limitations are not considered sufficient to patentably distinguish over the prior art.

5. Claims 7-21 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motorola "M68040 User's Manual" and Chauvel et al. (US App. Pub. No. 2002/0073282) in further view of Vishin et al. (5,860,146).

As per claims 7-21 and 40-43, being dependant on claim 1, 34, or those correspondingly dependant inclusively, as taught by Motorola and/or Chauvel et al., but does not teach that multiple MMU's may be cascaded thereby effectively enabling an initial virtual address to be first translated to an intermediate virtual address which may be utilized logically as if it were a physical address, but which is then further translated to a final physical address, thereby effectively enabling the intermediate virtual address to represent a virtualized physical address, so that a virtual address's final physical target may be conveniently remapped independently of any number processes whose virtual intermediate address that may reference it (i.e. enabling a logical physical target to be efficiently physically remapped). However Vishin et al. teaches this (figure 5, and lines 8-13). It would be obvious to one of ordinary skill in the art at the time of the disclosed invention to combine that taught by Motorola and Chauvel et al. with that taught by Vishin et al. relevant to these claims, for the benefit of enabling multiple independent processes to logically utilize a common virtual intermediate address as if it represented a final physical address to enable the final physical address to be remapped independently of the addresses managed local to the processes, and/or

Art Unit: 2186

corresponding supervisory process or operating system. Any and all potentially further remaining claimed limitations are not considered sufficient to patentably distinguish over the prior art.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


PIERRE BATAILLE
PRIMARY EXAMINER
12/09/05